V-Band 2-b and 4-b Low-Loss and Low-Voltage Distributed MEMS Digital Phase Shifter Using Metal–Air–Metal Capacitors

Hong-Teuk Kim, *Student Member, IEEE*, Jae-Hyoung Park, Sanghyo Lee, Seongho Kim, Jung-Mu Kim, Yong-Kweon Kim, *Member, IEEE*, and Youngwoo Kwon, *Member, IEEE*

***Abstract*—Low-loss digital distributed phase shifters have been developed using micromachined capacitive shunt switches for V-band applications. Instead of conventional metal–insulator–metal capacitors, high-Q metal–air–metal capacitors were used in series with the microelectromechanical system (MEMS) shunt capacitive switches to minimize the dielectric loss. The operation voltage for the phase shifters was also reduced by applying the bias directly to the MEMS shunt switches through choke spiral inductors. Fabricated 2-b (270°) and 4-b (337.5°) distributed phase shifters showed low average insertion losses of 2.2 dB at 60 GHz and 2.8 dB at 65 GHz, respectively. The average phase errors for 2-b and 4-b phase shifters were 6.5% and 1.3%, respectively. The return losses are better than 10 dB over a wide frequency range from 40 to 70 GHz. Most of the circuits operated at 15–35-V bias voltages. These phase shifters present promising solution to low-loss integrated phase shifting devices at the V-band and above.**

***Index Terms*—Broad-band, metal–air–metal (MAM) capacitor, micromachining technology, phase shifter.**

I. Introduction

ANALOG phase shifters using coplanar waveguide (CPW) lines with distributed microelectromechanical system (MEMS) bridges have recently demonstrated broad-band characteristics with low loss of 4.0 dB/360° at 60 GHz [1]. However, since there was a limit on the control range of the bridge height before the bridge snaps, the analog phase shifter showed relatively small phase shift. This problem was solved by operating the MEMS bridges in the digital mode [2]–[8], where two distinct capacitance states (ON: bridge snapped and OFF: bridge as is) were defined with a high $C_{\rm on}/C_{\rm off}$ ratio. Digital phase shifters with this approach allow large phase shift and low sensitivity to electrical noise. In the published CPW digital phase shifters [2], [3], a small metal–insulator–metal (MIM) capacitor in series with the MEMS bridge capacitor was used to reduce the total shunt capacitance seen by the line, resulting in an acceptable return loss for both switching states over a wide band. Here, the biasing to the MEMS capacitor was applied through these two series capacitors, resulting in high actuation bias voltages in excess of 40 V. If this approach were to be applied at higher frequencies such as the V-band, the bias voltage would be too high to be practical. This is due to the fact that the required MEMS shunt capacitance of the CPW lines decreases as frequency increases, making the switching voltage even higher. Moreover, the loss of the loaded CPW line will increase because of the low Q of the MIM capacitor at high frequencies [3]. The goal of this study was to realize a distributed CPW digital phase shifter with low loss and reasonable actuation voltage at V-band. In order to minimize the loss at V-band, metal–air–metal (MAM) capacitors in series with a MEMS capacitor were used for the shunt capacitors. The low capacitance per unit area and high-Q factor of the MAM capacitors make MAM capacitors better suited to V-band applications than MIM capacitors. MAM structures have previously been successfully employed to demonstrate the low-loss compact filters by the authors [9]. Also, a similar approach is employed to realize a low-loss distributed MEMS phase shifter at Ka-band [10]. In addition to the low-loss capability made possible by the MAM capacitors,

TABLE I
COMPARISON OF LOSS AND PULL-DOWN VOLTAGE FOR SEVERAL MEMS PHASE SHIFTERS

Reference	Type	Average Insertion Loss	Frequency	Pull-down Volt
[1]	CPW analog Distributed type (360°)	4 dB	60 GHz	> 13 V
[2]	CPW 1-bit Distributed type (270°)	1.69 dB	35 GHz	75 V
[3]	CPW 2-bit Distributed type (270°)	4 dB	11.4 GHz	60 V
[4]	CPW 3-bit Distributed type (315°)	1.7 dB	26 GHz	60 V
[5]	Microstrip 4-bit Distributed type (337°)	3 dB	16 GHz	40-60 V
[6]	Microstrip 4-bit Resonant Line (337°)	2.25 dB	34 GHz	45 V
[7]	Microstrip 4-bit True-Time Delay (337°)	2.5 dB	10.8 GHz	70 V
[8]	Microstrip 4-bit Reflection type (337°)	1.4 dB	8 GHz	35-40 V
This work	CPW 2-bit Distributed type (270°)	2.2 dB	60 GHz	15-20 V
This work	CPW 4-bit Distributed type (337°)	2.8 dB	65 GHz	25-35 V

Manuscript received April 5, 2002; revised August 23, 2002. This work was supported by the Korean Ministry of Science and Technology through the Creative Research Initiative Program.

The authors are with the Center for 3-D Millimeter-Wave Integrated Systems, School of Electrical Engineering, Seoul National University, Seoul 151-742, Korea (e-mail: ykwon@snu.ac.kr, htkim@snu.ac.kr).

Digital Object Identifier 10.1109/TMTT.2002.805285

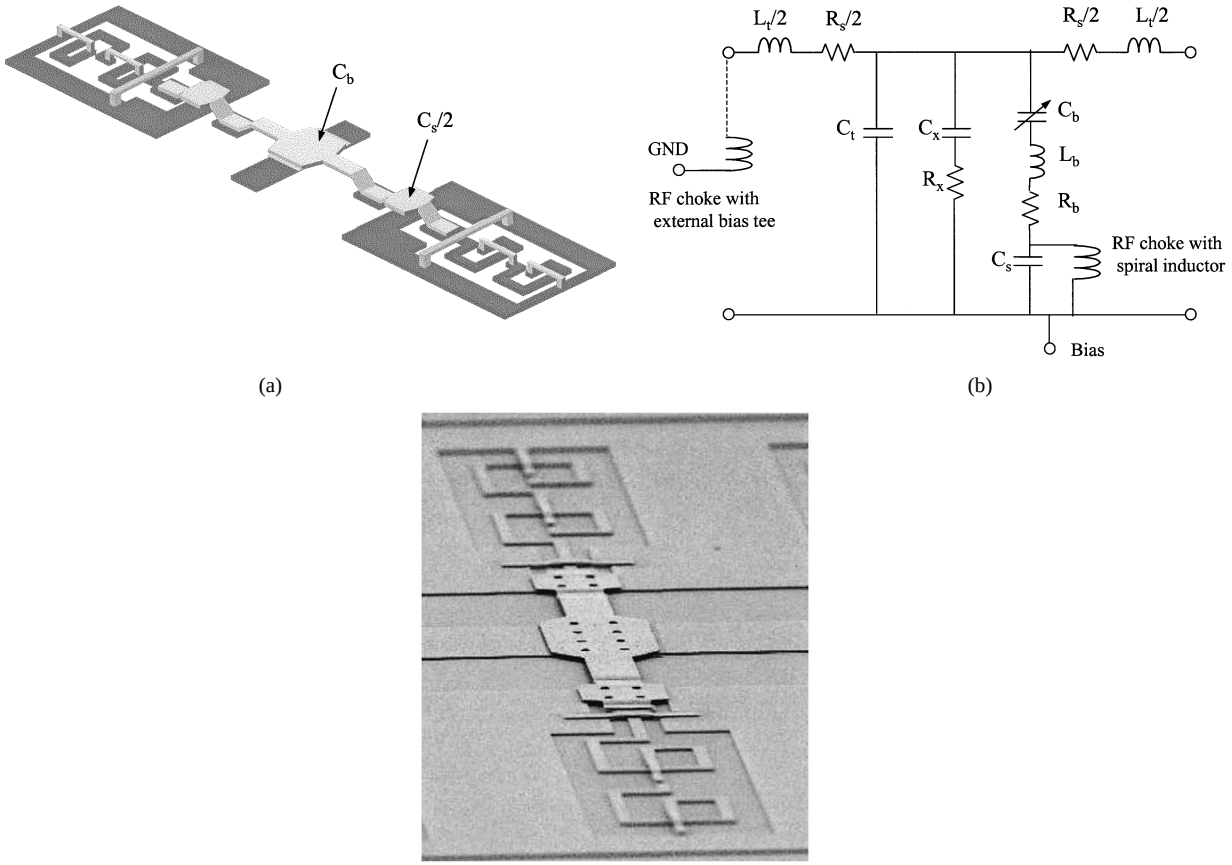


Fig. 1. (a) Schematic and (b) equivalent circuit (c) photograph of the unit cell of a phase shifter with MEMS bridge and series MAM capacitors.

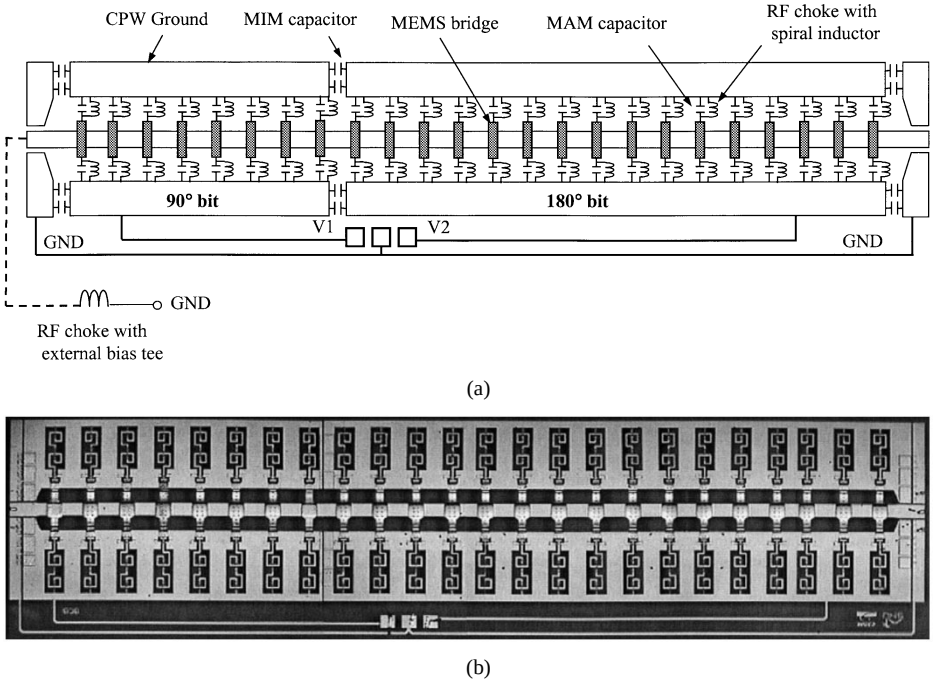


Fig. 2. (a) Diagram and (b) photograph of the fabricated V-band 2-b MEMS phase shifter. Chip size is 6.3 mm × 1.5 mm (24 bridges).

the bias voltage was also reduced in this study by employing choke spiral inductors in the bias circuit. In this way, the bias could be directly applied to the MEMS capacitors, bypassing the series MAM capacitors.

In this study, combining the aforementioned ideas to reduce the loss and bias voltages, 4-b as well as 2-b phase shifters have been designed at V-band and fabricated using the surface micromachining techniques. The measured loss and operation voltage

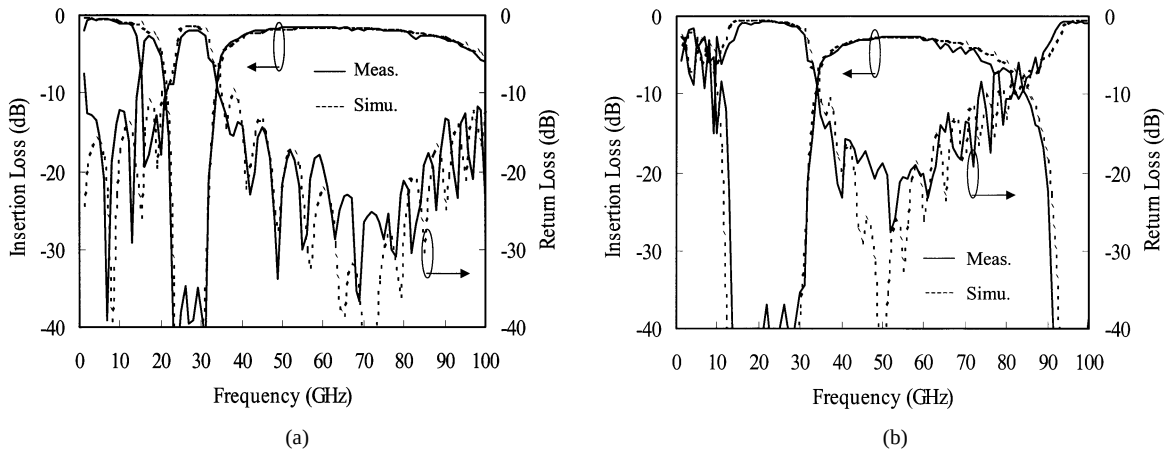


Fig. 3. Measured and simulated S-parameters of a 2-b MEMS phase shifter at (a) 0° phase shift and (b) 270° phase shift at 60 GHz.

of our phase shifters are compared with the reported MEMS phase shifters at various bands in Table I. It can be easily found from the table that the insertion losses and the bias voltages of our phase shifters compare very well even with the lower frequency phase shifters. To the best of our knowledge, this is the first demonstration of the low-loss broad-band digital MEMS phase shifters at V-band.

II. Design and Fabrication

The V-band digital MEMS distributed phase shifters of this study consist of a high-impedance CPW line ($Z_0 = 96\ \Omega$, $\mathrm{width} = 100\ \mu$m, $\mathrm{gap} = 120\ \mu$m) capacitively loaded by the periodic placement [2], [3] of a series-connected MEMS bridges and MAM capacitors. The unit cell of the digital distributed phase shifter is shown in Fig. 1 together with the equivalent circuit model. In this design, the range of the characteristic impedances was first chosen to be from 46 to 59 Ω to guarantee good impedance matching ($S_{11} < -13$ dB) up to 75 GHz. This requires an overall $C_{\mathrm{on}}/C_{\mathrm{off}}$ ratio of 1.6 (40/25 fF) seen by the line. The length of the unit cell is 262 μm. A 262-μm-long 96-Ω line was modeled with a shunt capacitance (C_t) of 5 fF, series inductance (L_t) of 104 pH, and series resister (R_s) of 0.1 Ω. The loaded capacitance seen by the line is the series combination of the MEMS bridge capacitance (C_b) and total MAM capacitance (C_s). The total capacitance (C_{off} or C_{on}) of the unit cell is

$$C_{\mathrm{off}} = C_t + \frac{C_s C_{\mathrm{bu}}}{(C_s + C_{\mathrm{bu}})} \text{ and}$$
$$C_{\mathrm{on}} = C_t + \frac{C_s C_{\mathrm{bd}}}{(\mathbf{C}_s + C_{\mathrm{bd}})} \quad (1)$$

where C_{bu} is MEMS bridge capacitance in the up-state position and C_{bd} in the down-state position.

Considering that the ON/OFF capacitive ratio ($C_{\mathrm{bd}}/C_{\mathrm{bu}}$) of the MEMS shunt capacitor switch with a 1.5-μm air gap was about 8 in our experiment, the bridge capacitance (C_{bu}) of 69 fF (100 μm × 102 μm) in the up-state and the fixed MAM capacitance ($C_s/2$) of 21 fF (62 μm×50 μm) were determined to meet the acceptable impedance matching up to 75 GHz. The total inductance (L_b) of bridge and MAM capacitors is 26 pH. The Bragg frequencies of the unit cell in the phase shifter are over 142 GHz for both switch states. In order to achieve a very small

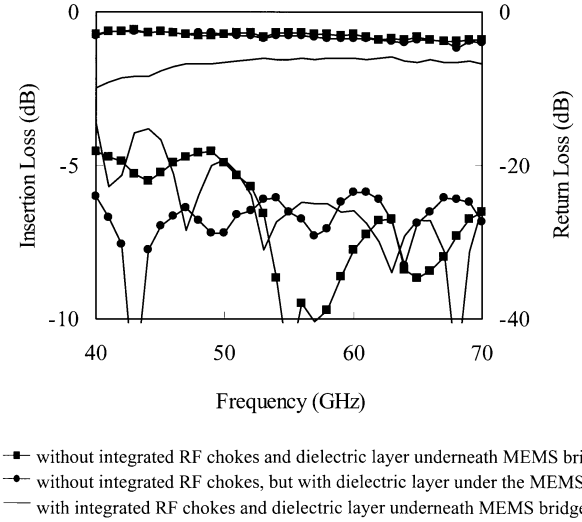
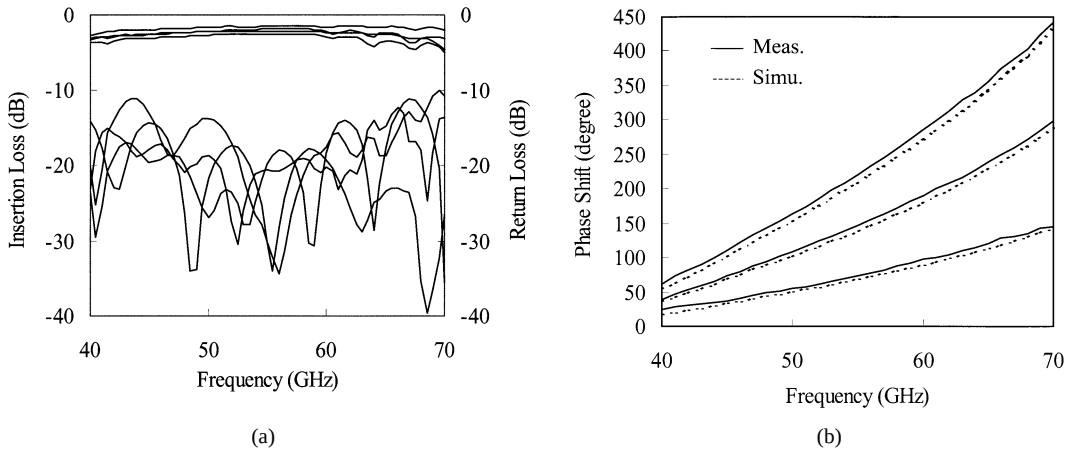


Fig. 4. Comparison of the measured losses due to the integrated RF chokes for biasing and dielectric layer underneath MEMS bridges for blocking dc short at a 2-b MEMS phase shifter.

fixed capacitance ($C_s/2$) of 21 fF, MAM capacitors were employed instead of MIM capacitors since they are less sensitive to the process variations compared with the latter. It also offers high-Q factors at high frequencies as required for V-band operation. The bias for switching is applied directly to the MEMS switch through the spiral inductors to reduce the switching dc voltage down to 20 V. Total inductance of two cascaded spiral inductor is 0.7 nH with self-resonance frequency higher than 87 GHz.

For modeling and analysis, most of the lumped element values were calculated using an electromagnetic (EM) simulator IE3D. However, some parameter values such as bridge conductor loss ($R_b = 0.3\ \Omega$) and the frequency-dependent losses ($C_x = 1.5$ fF and $R_x = 10000\ \Omega$) such as substrate loss, surface wave leakage loss, and radiation loss of the loaded line are determined by the measured S-parameters. The simulated phase shift of the unit cell is about 11.2° at 60 GHz. A circuit simulator ADS was used for the simulation of the whole phase-shifter circuit.

The phase shifters were fabricated on a 520-μm-thick quartz substrate ($\varepsilon_r = 3.8$). First, titanium and gold are thermally



(a) (b)

Fig. 5. Measured results of 2-b (270° at 60 GHz) MEMS phase shifter. (a) Insertion loss and return loss. (b) Phase shift.

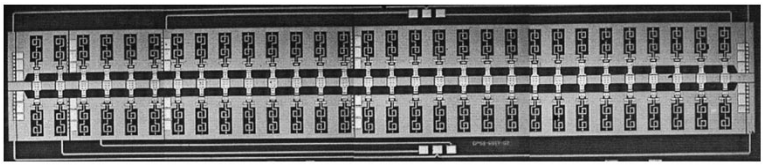


Fig. 6. Photograph of the fabricated V-band 4-b MEMS phase shifter. Chip size is 7.9 mm × 1.5 mm (30 bridges).

evaporated on the quartz substrate as a seed layer. An electroplating mold is formed using thick photoresist, through which 3-μm-thick gold transmission lines are electroplated. The gold electroplating process is carried out using commercially available noncyanide electrolytic solution (NEUTRONEX 210 B), and the electrolytic solution temperature is fixed at 60 °C. The electroplating rate is proportional to current density and electroplating time. The thickness of the electroplated structures can be controlled by varying the electroplating time at a fixed current density. In this study, the current density of the electroplating is fixed at 2 mA/cm^2 with the electroplating rate of 0.125 μm/min. In this case, the surface roughness (Ra) of the electroplated structure is 0.061 μm. After removing the electroplating mold, a 0.3-μm-thick silicon nitride (SiN) was deposited with plasma-enhanced chemical vapor deposition (PECVD) over the signal line under the bridges to avoid a dc voltage short when the bridge structure is deflected to the bottom ground plate. To form a sacrificial layer with the thickness of 1.5 μm for the 2-b design and 1.75 μm for the 4-b design, the photoresist is spin-coated and patterned by UV lithography. The patterned sacrificial layer is thermally cured to reflow the photoresist to the temperature of 200 °C. Next, the seed layer is evaporated and an electroplating mold is formed. After electroplating the overhanging bridge structures with gold, the sacrificial layer is ashed using a plasma process. The thickness of the bridge is 2.0 μm. The details of the fabrication technology have been reported in our previous paper [11].

III. Measurements

Fig. 2 shows the photograph of a V-band 2-b (270°) distributed MEMS phase shifter that consists of two 1-b phase shifters for 90° and 180° phase shift at 60 GHz. The chip size is 6.3 mm × 1.5 mm (24 bridges). DC bias for each 1-b phase shifter is connected to the ground pad of the CPW line while the signal line is connected to dc ground through the external bias tee. When dc bias is applied, the voltage difference between the signal line and ground pad generates a strong electric field under the membrane of the MEMS switch, which forces the membrane to snap down. DC block capacitors are added between the consecutive ground pads of 1-b phase shifter sections and also between the RF probe pads and the 1-b phase shifter sections so that the bias may be applied independently while keeping the RF ground plane continuity. The area of the dc block MIM capacitor is 80 μm × 140 μm and the thickness of SiN is 0.3 μm.

TABLE II
Phase Shift and Loss Data of the 2-b MEMS Phase Shifter at 60 GHz

Phase State	0.0º	90.0º	180.0º	270.0º
Measured	0.0º	97.2 º	189.8 º	285.2 º
Phase Error	0.0º	-7.2 º	-9.8 º	-15.2 º
Loss (dB)	1.5	2.3	2.7	2.3

RF measurements were made using a semi-automatic CASCADE probe station and HP 8510XF network analyzer, calibrated using line-reflect–reflect-match (LRRM) techniques with on-wafer standards. The actuation voltage for most of the MEMS switch is 15–20 V. Fig. 3 shows the measured and simulated S-parameters of the 2-b phase shifter for the two phase states; all the MEMS air-bridges of the phase shifter are up in the state of 0° phase shift [Fig. 3(a)] and are pulled down in the state of 270° phase shift [Fig. 3(b)]. The lumped-elements model of the phase shifter unit cell in Fig. 1(b) was used for this circuit simulation. For both phase states, the integrated spiral RF choke for biasing results in the band rejection characteristics near 20 GHz. However, broad-band impedance matching is observed over a wide passband ranging from 40 to 70 GHz with the return losses better than 10 dB. In Fig. 3, good agreement

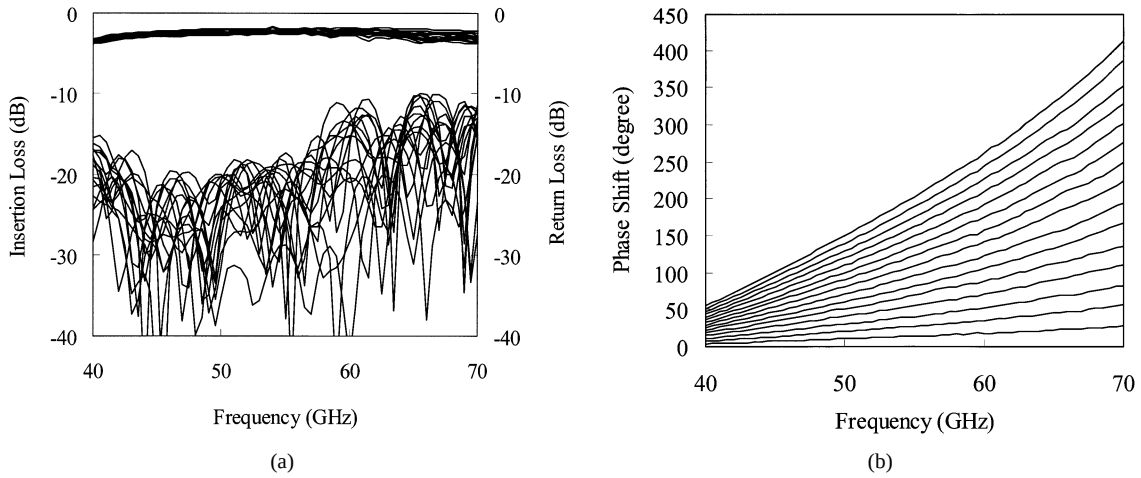


Fig. 7. Measured results of the 4-b (337.5° at 65 GHz) MEMS phase shifter. (a) Insertion loss and return loss. (b) Phase shift.

TABLE III
PHASE SHIFT AND LOSS DATA OF THE 4-BIT MEMS PHASE SHIFTER AT 65 GHz

Phase State	0.0°	22.5°	45.0°	67.5°	90.0°	112.5°	135.0 °	157.5°
Measured	0.0°	22.3°	45.2°	67.6°	90.8°	112.5	132.9 °	154.0°
Phase Error	0.0°	0.2 °	-0.2°	-0.1°	-0.8°	0.0°	2.1°	3.5 °
Loss (dB)	2.0	2.2	2.3	2.5	2.5	2.9	2.6	2.8
Phase State	180.0°	202.5°	225.0°	247.5°	270.0°	292.5°	315.0 °	337.5°
Measured	179.2°	200.5°	221.6°	244.5°	265.1°	284.6 °	307.9 °	329.2°
Phase Error	0.8°	2.5 °	3.4°	3.0°	4.9°	7.9°	7.1°	8.3 °
Loss (dB)	2.7	2.8	3.1	3.3	3.2	3.6	3.1	3.3

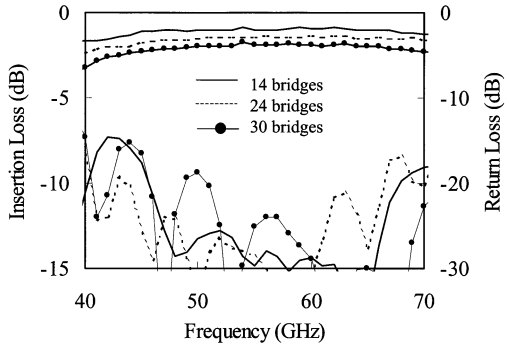


Fig. 8. Measured insertion losses of phase shifters with different numbers of MEMS bridges (14, 24, 30 bridges) when all MEMS bridges are up in the state of 0° phase shift.

between simulation and measurement validates the lumped model of Fig. 1(b) used in the phase shifter design. Fig. 4 shows the effects of the integrated spiral RF chokes and the 0.3-μm-thick SiN dielectric layer underneath MEMS bridges for avoiding a dc short. From the measured results of Fig. 4, the losses from the integrated spiral RF chokes and SiN layer are estimated to be 0.62 and 0.13 dB at 60 GHz, respectively.

Measured results of the 2-b (270°) phase shifter for all switching states are shown in Fig. 5. The return losses are better than 10 dB from 40 to 70 GHz and the average insertion loss is about 2.2 dB at 60 GHz. The measured average phase error for all switching states is 6.5% at 60 GHz. Detailed phase shift and loss data are listed in Table II.

Fig. 6 shows the photograph of the V-band 4-b (337.5°) distributed MEMS phase shifter with four 1-b phase shifters for 22.5°, 45°, 90°, and 180° phase shifts at 65 GHz. The chip size is 7.9 mm $\times$ 1.5 mm. The 4-b phase shifter was fabricated with a 1.75-μm air-gap, which resulted in the increase of the actuation voltages. The switching voltage was 25–35 V for the 4-b design. Fig. 7(a) shows the insertion and return losses of the 4-b phase shifter at each phase state. The return losses for all 16 switching states are better than 10 dB from 40 to 70 GHz and the average insertion loss is about 2.8 dB at 65 GHz. Fig. 7(b) illustrates the frequency-dependent phase shift for all 16 switching states. The measured average phase error for all switching states is 1.3% at 65 GHz. Detailed phase shift and loss data are listed in Table III. In order to estimate the loss of each unit cell, phase shifters with three different numbers of unit cells were fabricated as test structures. Fig. 8 shows the measured loss of phase shifters with different numbers of MEMS bridges (14, 24, 30 bridges) when all MEMS bridges are up in the state of 0° phase shift. The loss of the phase shifters increases according to numbers of MEMS bridges and the corresponding losses at 60 GHz are 0.9, 1.5, and 1.6 dB, respectively. In this case, the loss can be represented as

$$\text{Loss (dB)} \approx 0.063 \times N \tag{2}$$

where N is the number of MEMS bridges.

In other words, the loss of the unit cell in our design was 0.063 dB, which agrees well with the simulated loss of 0.06 dB.

IV. CONCLUSION

Two-bit and 4-b low-loss distributed digital MEMS phase shifters have been designed, fabricated, and tested for the first time at V-band. By direct biasing to the bridge membranes through the spiral choke inductors, the MEMS phase shifter operates at reasonable switching voltages of 15–35 V. In addition, the loss of the MEMS phase shifter was reduced through the use of high-Q MAM capacitors instead of the conventional MIM capacitor. Minimization of the dielectric loss in the loaded lines resulted in low average insertion loss of 2.2 dB/2-b (270°) at 60 GHz and 2.8 dB/4-b (337°) at 65 GHz. The phase error of

the 4-b design is as small as 1.3% at 65 GHz. Low-loss and low-voltage operation of this study opens a new possibility of low-loss phase shifting devices at V-band and above.

REFERENCES

[1] N. S. Barker and G. M. Rebeiz, "Optimization of distributed MEMS transmission-line phase shifters—U-band and W-band designs," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1957–1966, Nov. 2000.

[2] A. Borgioli, Y. Liu, A. S. Nagra, and R. A. York, "Low-loss distributed MEMS phase shifter," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 7–9, Jan. 2000.

[3] J. S. Hayden and G. M. Rebeiz, "2-bit MEMS distributed X-band phase shifters," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 540–542, Dec. 2000.

[4] Y. Liu, A. Borgioli, A. S. Nagra, and R. A. York, "K-band 3-bit low-loss distributed MEMS phase shifter," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 415–417, Oct. 2000.

[5] J. S. Hayden, A. Makczewski, J. Kleber, C. L. Goldsmith, and G. M. Rebeiz, "2 and 4-bit DC-18 GHz microstrip MEMS distributed phase shifters," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001, pp. 219–222.

[6] B. Pillans, S. Eshelman, A. Malczewski, J. Ehmke, and C. L. Goldsmith, "Ka-band RF MEMS phase shifters," *IEEE Microwave Guided Wave Lett.*, vol. 9, pp. 520–522, Dec. 1999.

[7] M. Kim, J. B. Hacker, R. E. Mihailovich, and J. F. DeNatale, "A DC-to-40 GHz four-bit RF MEMS true-time delay network," *IEEE Microwave Wireless Comp. Lett.*, vol. 11, pp. 56–58, Feb. 2001.

[8] A. Malczewski, S. Eshelman, B. Pillans, J. Ehmke, and C. L. Goldsmith, "X-band RF MEMS phase shifters for phased array applications," *IEEE Microwave Guided Wave Lett.*, vol. 9, pp. 517–519, Dec. 1999.

[9] H. T. Kim, J. H. Park, Y. K. Kim, and Y. Kwon, "Compact low-loss monolithic CPW filters using air-gap overlay structures," *IEEE Microwave Wireless Comp. Lett.*, vol. 11, pp. 328–330, Aug. 2001.

[10] J. S. Hayden and G. M. Rebeiz, "A low-loss Ka-band distributed MEMS 2-bit phase shifter using metal–air–metal capacitors," in *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 337–340.

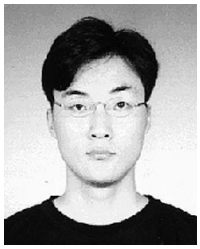
[11] J. H. Park, H. T. Kim, K. Kang, Y. Kwon, and Y. K. Kim, "A micromachined millimeter wave phase shifter using semi-lumped elements," in *Proc. 11th Int. Solid-State Sens. Actuators Transducers Conf.*, June 2001, pp. 1552–1555.

Hong-Teuk Kim (S'99) was born in Pusan, Korea, in 1968. He received the B.S. degree from the Pusan National University, Pusan, Korea, in 1991, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, in 1993, and is currently working toward the Ph.D. degree at the Seoul National University, Seoul, Korea.

From 1993 to 1998, he was with the LG Central Institute of Technology (LGCIT), where he was engaged in low-noise system integration and superconductor RF filter design for wireless application. His current research is focused on MMIC design, RF MEMS design, and analysis of oscillator phase noise.

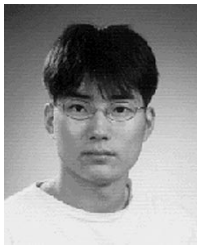
Jae-Hyoung Park was born in Korea, in 1975. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Seoul National University, Seoul, Korea, in 1997, 1999, and 2002, respectively.

He is currently a Post-Doctoral Researcher with the Inter-University Semiconductor Research Center (ISRC), Seoul National University. He is also a Member of Research Staff for the development of micromachined millimeter-wave device with the Center for 3-D Millimeter-Wave Integrated Systems, Seoul National University. From 1997 to 1998, his main research activities were the manipulation of microparticles. Since 1998, his research interests are focused on the design and fabrication of RF/millimeter-wave MEMS devices.



Sanghyo Lee received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 2000 and 2002, respectively, and is currently working toward the Ph.D. degree in electrical engineering and computer science at the Seoul National University.

He is currently with the 3-D Millimeter-Wave Integrated Systems (C3DM) Group, Seoul National University. From 2000 to 2002, his main research activities were the active device modeling and RF MEMS device development. His current research interests are mainly focused on the design of RF MEMS devices and the embodiment of three-dimensional millimeter-wave beam steering subsystems integrated with active MMICs.



Seongho Kim was born in Jeonnam, Korea. He received the B.S. degree in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2001, and is currently working toward the M.S. degree at the Seoul National University.

His current research is focused on the modeling of solid-state devices in millimeter-wave region.

Jung-Mu Kim received the B.S. degree from Ajou University, Suwon, Korea, in 2000, the M.S. degree from the Seoul National University, Seoul, Korea, in 2002, and is currently working toward the Ph.D. degree in electrical engineering and computer science at the Seoul National University.

He is currently with the RF MEMS Group, Micro Sensors and Actuators (MiSA) Laboratory, Seoul National University. From 2000 to 2002, his main research activities were the surface modification for RF MEMS device. His current research interests are mainly focused on the design and fabrication of RF MEMS devices, including surface modification and wet release process.

Yong-Kweon Kim (S'90–M'90) received the B.S. and M.S. degrees in electrical engineering from the Seoul National University, Seoul, Korea, in 1983 and 1985, respectively, and the Dr. Eng. degree from the University of Tokyo, Tokyo, Japan, in 1990. His doctoral dissertation concerned modeling, design, fabrication, and testing of microlinear actuators in magnetic levitation using high critical temperature superconductors.

In 1990, he joined the Central Research Laboratory of Hitachi Ltd., Tokyo, Japan, as a Researcher, where he was involved with actuators of hard disk drives. In 1992, he joined the Seoul National University, where he is currently an Associate Professor in the School of Electrical Engineering. His current research interests are modeling, design, fabrication, and testing of electric machines, especially MEMS, microsensors, and actuators.

Youngwoo Kwon (S'90–M'94) was born in Korea, in 1965. He received the B.S. degree in electronics engineering from the Seoul National University, Seoul, Korea, in 1988, and the M.S. and Ph.D. degrees in electrical engineering from The University of Michigan at Ann Arbor, in 1990 and 1994, respectively.

From 1994 to 1996, he was with the Rockwell Science Center, where he was involved in the development of various millimeter-wave monolithic integrated circuits based on HEMTs and HBTs. In 1996, he joined the faculty of the School of Electrical Engineering, Seoul National University. His current research activities include the design of MMICs for mobile communication and millimeter-wave systems, large-signal modeling of microwave transistors, application of micromachining techniques to millimeter-wave systems, nonlinear noise analysis of MMICs, and millimeter-wave power combining.